

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1 1. (Amended) A charge coupled device (CCD) imaging
2 apparatus comprising:

3 a CCD operable infor a progressive scanning mode;

4 a drive pulse switching circuit for generating a CCD read~~drive~~ pulse
5 ~~for said CCD~~ at a first frame rate, and for generating a CCD drive pulse at a
6 second frame rate being $n/2$ times the first frame rate, n being an integer;

7 a CCD driver for driving said~~the~~ CCD ~~by converting the CCD drive~~
8 ~~pulse into a specified voltage;~~

9 a frame memory for storing an output signal of said CCD in one frame
10 after the CCD read pulse, and for reading out the stored output signal of said
11 CCD $n/2$ times; and

12 a camera signal processing circuit for receiving an output signal of
13 said frame memory and performing a ~~specified~~ camera process.,

14 ~~wherein said drive pulse switching circuit generates a CCD read pulse~~
15 ~~of the CCD drive pulse at the first frame rate, and generates the CCD drive~~
16 ~~pulse other than the CCD read pulse at a frame rate $(n/2)$ times as high as the~~
17 ~~first frame rate, the n being an arbitrary integer, and~~

18 ~~wherein said frame memory stores an output signal of said CCD in~~
19 ~~one frame right after the CCD read pulse, and repeats to read out the stored~~
20 ~~output signal of said CCD in one frame $(n/2)$ times.~~

1 3. (Amended) The CCD imaging apparatus of claim 2, further
2 comprising a first reproduced signal converter being capable offor outputting a
3 reproduced signal of said recorder unit ~~selectively at the frame rate $(n/2)$ times~~

4 ~~as high as the first frame rate and at the first and second frame rates~~rate.

1 4. (Amended) The CCD imaging apparatus of claim 3, further
2 comprising:

3 a viewfinder for displaying ~~a~~an output signal of said camera signal
4 processing circuit; and

5 a second reproduced signal converter for converting the reproduced
6 signal from said recorder unit to the second frame rate ~~(n/2) times as high as~~
7 ~~the first frame rate~~, and for outputting the converted signal to said viewfinder.

1 5. (Amended) The CCD imaging apparatus of claim 1,

2 wherein, when the first frame rate is below~~lower than~~ a specified
3 number~~frame rate~~, said drive pulse switching circuit generates the CCD read
4 pulse for said CCD at the first frame rate, and generates the CCD drive pulse
5 ~~other than the CCD read pulse~~ at the second frame rate ~~(n/2) times as high as~~
6 ~~the first frame rate~~, and

7 wherein, when the first frame rate is below~~lower than~~ the specified
8 number~~frame rate~~, said frame memory stores the output signal of said CCD ~~in~~
9 ~~one frame right~~ after the CCD read pulse, and ~~repeats to reads~~ out the stored
10 output signal of said CCD ~~in one frame~~ ~~(n/2)~~ times.

1 6. (Amended) The CCD imaging apparatus of claim 5, wherein
2 the specified number~~frame rate~~ is 30 frames/sec.

1 7. (Amended) The CCD imaging apparatus of claim 6, wherein
2 the first frame rate ~~is can be set at~~ 24 frames/sec, 25 frames/sec, or~~and~~ 30
3 frames/sec, and ~~the n~~ is 2.

1 8. (Amended) The CCD imaging apparatus of claim 1,

2 wherein said drive pulse switching circuit includes a frame rate

3 equalizing controller for ~~enabling~~making said CCD to output both a signal of
4 the first frame rate and a signal of a ~~third~~second frame rate at the ~~second~~a
5 ~~common~~ frame rate, the second frame rate being ~~of a common multiple of the~~
6 first and ~~third~~second frame rates, ~~and wherein said pulse switching circuit~~
7 ~~generates the other CCD drive pulse than the CCD read pulse for said CCD at~~
8 ~~the common frame rate.~~

1 9. (Amended) The CCD imaging apparatus of claim 8, wherein
2 the ~~second~~common frame rate ~~is can be set to~~ 60 frames/sec ~~or~~and 48
3 frames/sec.

1 10. (Amended) The CCD imaging apparatus of claim 9, further
2 comprising a recorder unit for recording a signal from said camera signal
3 processing circuit at the first and ~~third~~second frame rates.

1 11. (Amended) The CCD imaging apparatus of claim 10, wherein
2 said recorder unit reproduces a signal at the ~~second~~common frame rate.

1 12. (Amended) The CCD imaging apparatus of claim 10, further
2 comprising a first reproduced signal converting circuit for issuing a
3 reproduced signal of said recorder unit ~~selectively at the frame rate (n/2) times~~
4 ~~as high as the first frame rate and at the first and second frame rates~~rate.

1 14. (Amended) The CCD imaging apparatus of claim 1,
2 wherein said CCD is of a multiple frame interline transfer (MFIT)
3 type for reading out a progressive scanning signal divided into ~~an odd line~~
4 ~~field and an even line field~~fields,

5 wherein said frame memory outputs the signal in one frame in a
6 segment frame (SF) format by dividing the signal into ~~an odd line field and an~~
7 ~~even line field~~ fields,

8 wherein said drive pulse switching circuit comprises a read field
9 controller for generating a CCD drive pulse to control an order of ~~signals in~~

10 the odd and even fields being output from said CCD, and for

11 ~~wherein said read field controller changes~~ changing the order of the
12 ~~signals in the odd and even fields from said CCD every one frame when the n~~
13 ~~is an odd number at every frame, and~~

14 ~~wherein said read field controller does not change the order of the~~
15 ~~signals in the odd and even fields from said CCD when the n is an even~~
16 ~~number.~~

1 15. (Amended) A charge coupled device (CCD) imaging
2 apparatus comprising:

3 a CCD operable infor a progressive scanning mode;

4 a drive pulse switching circuit for generating a CCD read~~drive~~ pulse
5 ~~for said CCD~~ at a first frame rate, and for generating a CCD drive pulse at a
6 second frame rate being n/2 times the first frame rate, n being an integer;

7 a CCD driver for driving said CCD ~~by converting the CCD drive pulse~~
8 ~~into a specified voltage;~~

9 a camera signal processing circuit for receiving an output signal of
10 said CCD and performing a ~~specified~~ camera process;

11 a first frame memory for storing a first signal issued from said camera
12 signal processing circuit in one frame after the CCD read pulse, and for
13 reading out the stored first signal at a frame rate of the first signal n/2 times;
14 and

15 a second frame memory for storing the first signal and reading out the
16 stored first signal at the first frame rate, a reading out period of the first signal
17 being n/2 frames.

18 ~~wherein said drive pulse switching circuit generates a CCD read pulse~~

19 ~~of the CCD drive pulse at the first frame rate, and generates the CCD drive~~
20 ~~pulse other than the CCD read pulse at a frame rate $(n/2)$ times as high as the~~
21 ~~first frame rate, the n being an arbitrary integer,~~

22 ~~said first frame memory stores a signal in one frame of the first signal~~
23 ~~issued from said camera signal processing circuit right after the CCD read~~
24 ~~pulse, and repeats to read out the stored first signal $(n/2)$ times, and~~

25 ~~said second frame memory stores the first signals, and read out the~~
26 ~~stored first signal during a period of $(n/2)$ frames.~~

1 16. (Amended) The CCD imaging apparatus of claim 15, wherein
2 said second frame memory increases a number of samples in a horizontal
3 blanking period of the first signal, ~~and reads out the first signal during the~~
4 ~~period of $(n/2)$ frames.~~

1 17. (Amended) The CCD imaging apparatus of claim 15, further
2 comprising a recorder unit for recording and reproducing a signal issued from
3 said second frame memory at a rate of the signal issued from said second
4 frame memory.

1 19. (Amended) The CCD imaging apparatus of claim 15,

2 wherein, when the first frame rate is below ~~lower than~~ a specified
3 number frame rate, said drive pulse switching circuit generates the CCD read
4 pulse ~~for said CCD~~ at the first frame rate, and generates the CCD drive pulse
5 ~~other than the CCD read pulse~~ at the second frame rate $(n/2)$ times as high as
6 ~~the first frame rate,~~

7 wherein, when the first frame rate is below ~~lower than~~ the specified
8 number frame rate, said first frame memory stores the first signal, and ~~repeats~~
9 ~~to reads~~ read out the stored first signal $(n/2)$ times, and

10 wherein, when the first frame rate is below ~~lower than~~ the specified
11 number frame rate, said second frame memory stores the first signal, and the

12 ~~read~~ reads out ~~period of the stored first signal~~ during a period of $(n/2)$
13 frames.

1 20. (Amended) The CCD imaging apparatus of claim 19, wherein
2 the specified number~~frame rate~~ is 30 frames/sec.

1 21. (Amended) The CCD imaging apparatus of claim 20, wherein
2 the first frame rate ~~is~~ can be set at 24 frames/sec, 25 frames/sec, or ~~and~~ 30
3 frames/sec, and ~~the~~ n is 4.

1 22. (Amended) The CCD imaging apparatus of claim 1514,
2 further comprising a first reproduced signal converter being capable of ~~for~~
3 issuing a reproduced signal of said recorder unit ~~selectively at the frame rate~~
4 ~~$(n/2)$ times as high as the first frame rate and at the first and second frame~~
5 rate~~rate~~.

1 23. (Amended) The CCD imaging apparatus of claim 22, further
2 comprising a second reproduced signal converter for converting a reproduced
3 signal of said recorder unit to ~~a signal of the~~ second frame rate ~~$(n/2)$ times as~~
4 ~~high as the first frame rate~~, and

5 a switching circuit for ~~selectively~~ issuing outputs of said first frame
6 memory and said second reproduced signal converter.

1 24. (Amended) The CCD imaging apparatus of claim 1514,
2 further comprising a power on/off circuit for turning off said camera signal
3 processing circuit while~~except a period when~~ said camera signal processing
4 circuit does not output~~outputs~~ the first signal.